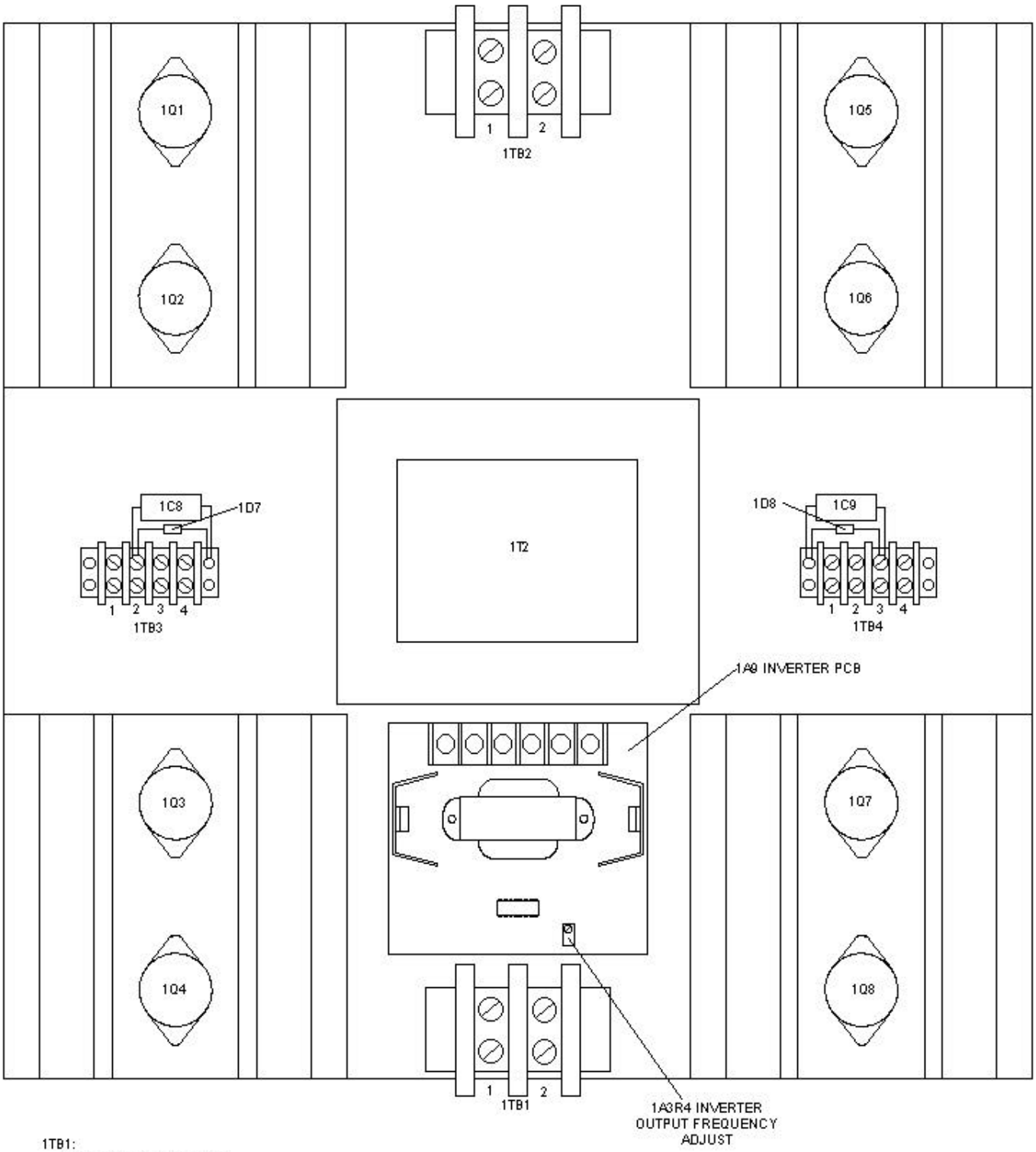

1TB1:
- Pin 1: Battery Neg Terminal
- Pin 2: Battery Pos Terminal

1TB2:
- Pin 1: Inverter Output (Hot) To 1A3TB1-3
- Pin 2: Inverter Output (Nuetral) To 1A3TB1-2

1TB3:
- Pin 1: Q1, Q2 Emitter
- Pin 2: Q1, Q2, Q3, Q4 Collector
- Pin 3: Q3, Q4 Emitter
- Pin 4: Q1, Q2, Q3, Q4 Base

1TB4:
- Pin 1: Q5, Q6, Q7, Q8 Base
- Pin 2: Q5, Q6 Emitter
- Pin 3: Q5, Q6, Q7, Q8 Collector
- Pin 4: Q7, Q8 Emitter

DRAWING TITLE	Inverter Chassis Diagram		
LOCATION	116 S. Prairie Ave. Waukegan, IL. 60085		
PROJECT NO. 001		DRAWN BY: John R. Schmitz	13 Jun 98
SCALE: None		DOC NAME: Inv Chassis.drw	
Power Backup System		DOC LOCATION: G:\John\Power Backup	
		DRAWING NO. SCH-001-023	REV O